6.4 Thermal Information

THERMAL METRIC[1]		LM1086			UNIT
		KTT	NDE	NGN	
		3 PINS	3 PINS	8 PINS	
R_{JA}	Junction-to-ambient thermal resistance	40.8	23.0	35.9	°C/W
$R_{JC(top)}$	Junction-to-case (top) thermal resistance	42.3	16.1	24.2	
R_{JB}	Junction-to-board thermal resistance	23.3	4.5	13.2	
ψ_{JT}	Junction-to-top characterization parameter	10.2	2.4	0.2	
ψ_{JB}	Junction-to-board characterization parameter	22.3	2.5	13.3	
$R_{JC(bot)}$	Junction-to-case (bottom) thermal resistance: Control Section/Output Section	1.5/4.0	1.5/4.0	2.9	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

Typicals and limits appearing in normal type apply for T_J = 25°C unless specified otherwise.

PARAMETER		TEST CONDITIONS	T_J = 25°C			T_J over the entire range for operation (see ***Recommended Operating Conditions***)			UNIT
			MIN	TYP	MAX	MIN[1]	TYP[2]	MAX[1]	
V_{REF}	Reference Voltage	LM1086-ADJ, I_{OUT} = 10 mA, $V_{IN} - V_{OUT}$ = 3 V, 10 mA ≤ $I_{OUT} \le I_{FULL\ LOAD}$, 1.5 V ≤ $V_{IN} - V_{OUT}$ ≤ 15 V[3]	1.238	1.250	1.262	1.225	1.250	1.270	V
V_{OUT}	Output Voltage[3]	LM1086-1.8, I_{OUT} = 0 mA, V_{IN} = 5 V, 0 ≤ $I_{OUT} \le I_{FULL\ LOAD}$, 3.3 V ≤ V_{IN} ≤ 18 V	1.782	1.8	1.818	1.764	1.8	1.836	V
		LM1086-2.5, I_{OUT} = 0 mA, V_{IN} = 5 V, 0 ≤ $I_{OUT} \le I_{FULL\ LOAD}$, 4.0 V ≤ V_{IN} ≤ 18 V	2.475	2.50	2.525	2.450	2.50	2.55	V
		LM1086-3.3, I_{OUT} = 0 mA, V_{IN} = 5 V, 0 ≤ $I_{OUT} \le I_{FULL\ LOAD}$, 4.75 V ≤ V_{IN} ≤ 18 V	3.267	3.300	3.333	3.235	3.300	3.365	V
		LM1086-5.0, I_{OUT} = 0 mA, V_{IN} = 8 V, 0 ≤ $I_{OUT} \le I_{FULL\ LOAD}$, 6.5 V ≤ V_{IN} ≤ 20 V	4.950	5.000	5.050	4.900	5.000	5.100	V
ΔV_{OUT}	Line Regulation[4]	LM1086-ADJ, I_{OUT} =10 mA, 1.5 V ≤ (V_{IN} - V_{OUT}) ≤ 15 V		0.015%	0.2%		0.035%	0.2%	
		LM1086-1.8, I_{OUT} = 0 mA, 3.3 V ≤ V_{IN} ≤ 18 V		0.3	6		0.6	6	mV
		LM1086-2.5, I_{OUT} = 0 mA, 4.0 V ≤ V_{IN} ≤ 18 V		0.3	6		0.6	6	mV
		LM1086-3.3, I_{OUT} = 0 mA, 4.5 V ≤ V_{IN} ≤ 18 V		0.5	10		1.0	10	mV
		LM1086-5.0, I_{OUT} = 0 mA, 6.5 V ≤ V_{IN} ≤ 20 V		0.5	10		1.0	10	mV

(1) All limits are specified by testing or statistical analysis.
(2) Typical Values represent the most likely parametric norm.
(3) $I_{FULL\ LOAD}$ is defined in the current limit curves. The $I_{FULL\ LOAD}$ Curve defines current limit as a function of input-to-output voltage. Note that 15W power dissipation for the LM1086 is only achievable over a limited range of input-to-output voltage.
(4) Load and line regulation are measured at constant junction temperature, and are specified up to the maximum power dissipation of 15W. Power dissipation is determined by the input/output differential and the output current. Ensured maximum power dissipation will not be available over the full input/output range.

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Electrical Characteristics (continued)

Typicals and limits appearing in normal type apply for T_J = 25°C unless specified otherwise.

PARAMETER		TEST CONDITIONS	T_J = 25°C			T_J over the entire range for operation (see ***Recommended Operating Conditions***)			UNIT
			MIN	TYP	MAX	MIN (1)	TYP (2)	MAX (1)	
ûV$_{OUT}$	Load Regulation (4)	LM1086-ADJ, (V_{IN}-V_{OUT}) = 3 V, 10 mA ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$		0.1%	0.3%		0.2%	0.4%	
		LM1086-1.8, 2.5, V_{IN} = 5 V, 0 ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$		3	12		6	20	mV
		LM1086-3.3, V_{IN} = 5 V, 0 ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$		3	15		7	25	mV
		LM1086-5.0, V_{IN} = 8 V, 0 ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$		5	20		10	35	mV
	Dropout Voltage (5)	LM1086-ADJ, 1.8, 2.5, 3.3, 5, ûV$_{REF}$, ûV$_{OUT}$ = 1%, I_{OUT} = 1.5A					1.3	1.5	V
I_{LIMIT}	Current Limit	LM1086-ADJ, V_{IN} − V_{OUT} = 5 V, V_{IN} − V_{OUT} = 25 V				1.50	2.7		A
						0.05	0.15		
		LM1086-1.8,2.5, 3.3, V_{IN} = 8 V				1.5	2.7		A
		LM1086-5.0, V_{IN} = 10 V				1.5	2.7		A
	Minimum Load Current (6)	LM1086-ADJ, V_{IN} −V_{OUT} = 25 V					5.0	10.0	mA
	Quiescent Current	LM1086-1.8, 2.5, V_{IN} ≤ 18 V					5.0	10.0	mA
		LM1086-3.3, V_{IN} ≤ 18 V					5.0	10.0	mA
		LM1086-5.0, V_{IN} ≤ 20 V					5.0	10.0	mA
	Thermal Regulation	T_A = 25°C, 30ms Pulse		0.008	0.04				%/W
	Ripple Rejection	f_{RIPPLE} = 120 Hz, C_{OUT} = 25 µF Tantalum, I_{OUT} = 1.5 A							dB
		LM1086-ADJ, C_{ADJ} = 25 µF, (V_{IN}− V_O) = 3 V				60	75		
		LM1086-1.8, 2.5, V_{IN} = 6 V				60	72		dB
		LM1086-3.3, V_{IN}= 6.3 V				60	72		dB
		LM1086-5.0 V_{IN} = 8 V				60	68		dB
	Adjust Pin Current	LM1086		55				120	µA
	Adjust Pin Current Change	10 mA ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$, 1.5 V ≤ (V_{IN}−V_{OUT}) ≤ 15 V					0.2	5	µA
	Temperature Stability						0.5%		
	Long Term Stability	T_A = 125°C, 1000 Hrs		0.3%	1.0%				
	RMS Noise (% of V_{OUT})	10 Hz ≤ f≤ 10 kHz		0.003%					

(5) Dropout voltage is specified over the full output current range of the device.
(6) The minimum output current required to maintain regulation.

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6.6 Typical Characteristics

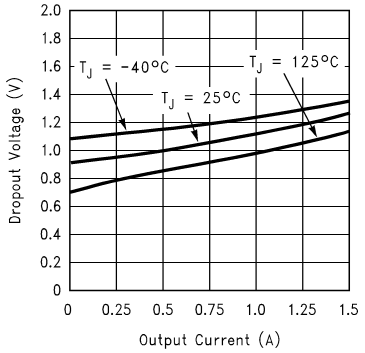

Figure 1. Dropout Voltage vs Output Current

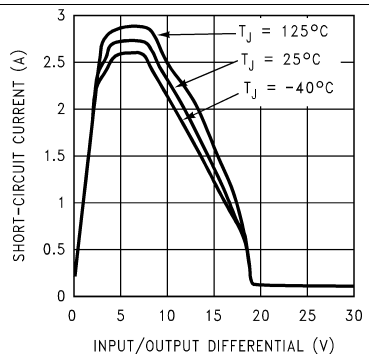

Figure 2. Short-Circuit Current vs Input/Output Difference

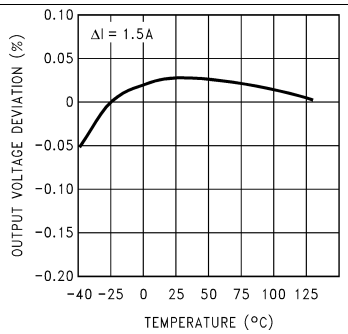

Figure 3. Load Regulation vs Temperature

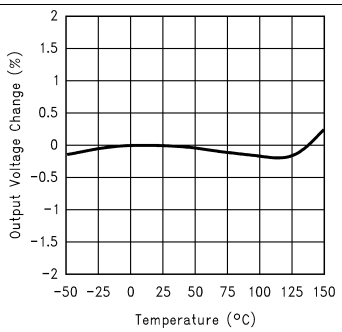

Figure 4. Percent Change in Output Voltage vs Temperature

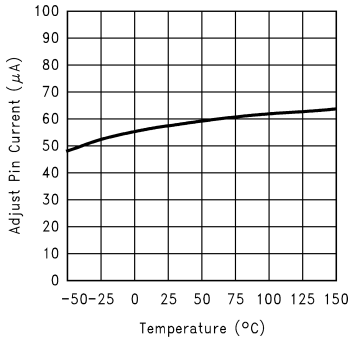

Figure 5. Adjust Pin Current vs Temperature

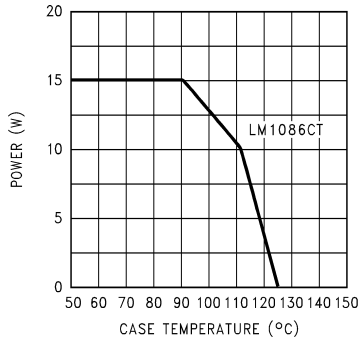

Figure 6. Maximum Power Dissipation vs Temperature

Typical Characteristics (continued)

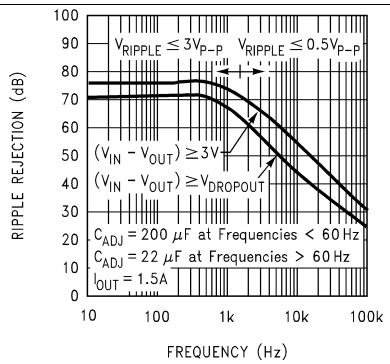

Figure 7. Ripple Rejection vs Frequency (LM1086-ADJ)

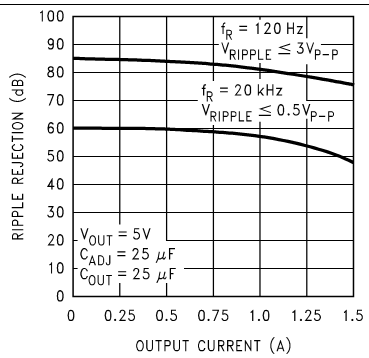

Figure 8. Ripple Rejection vs Output Current (LM1086-ADJ)

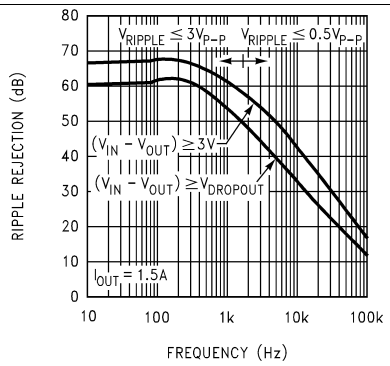

Figure 9. Ripple Rejection vs Frequency (LM1086-5)

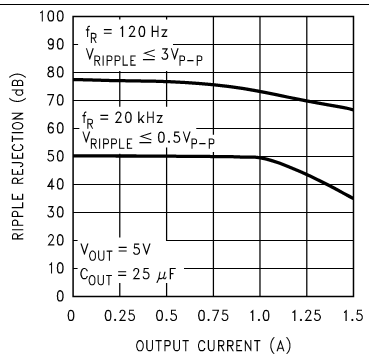

Figure 10. Ripple Rejection vs Output Current (LM1086-5)

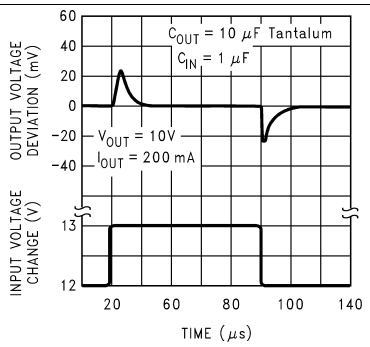

Figure 11. Line Transient Response

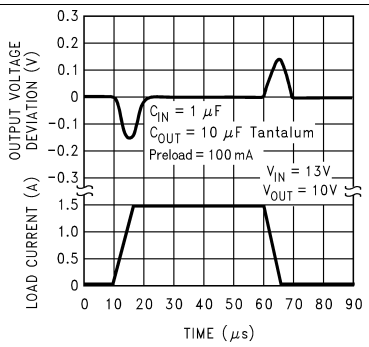

Figure 12. Load Transient Response

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7 Detailed Description

7.1 Overview

A basic functional diagram for the LM1086-ADJ (excluding protection circuitry) is shown in Figure 13. The topology is basically that of the LM317 except for the pass transistor. Instead of a Darlingtion NPN with its two diode voltage drop, the LM1086 uses a single NPN. This results in a lower dropout voltage. The structure of the pass transistor is also known as a quasi LDO. The advantage of a quasi LDO over a PNP LDO is its inherently lower quiescent current. The LM1086 is specified to provide a minimum dropout voltage of 1.5V over temperature, at full load.

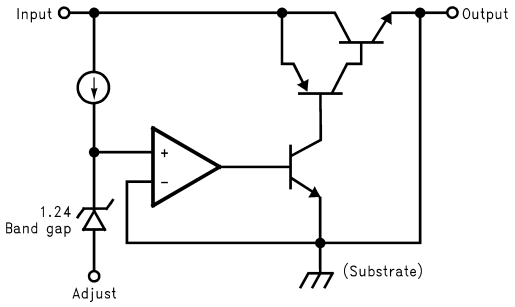
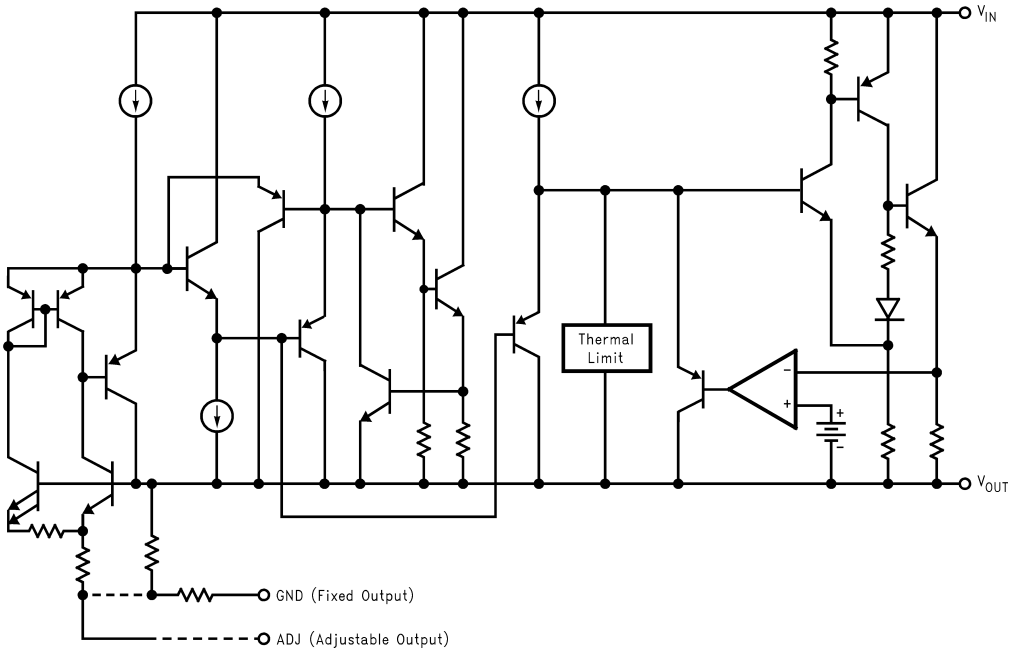


Figure 13. Basic Functional Block Diagram

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Ripple Rejection

Ripple rejection is a function of the open loop gain within the feed-back loop (refer to Figure 13 and Figure 16). The LM1086 exhibits 75dB of ripple rejection (typ.). When adjusted for voltages higher than V_{REF}, the ripple rejection decreases as function of adjustment gain: (1+R1/R2) or V_O/V_{REF}. Therefore a 5-V adjustment decreases ripple rejection by a factor of four (−12dB); Output ripple increases as adjustment voltage increases.

However, the adjustable version allows this degradation of ripple rejection to be compensated. The adjust terminal can be bypassed to ground with a capacitor (C_{ADJ}). The impedance of the C_{ADJ} should be equal to or less than R1 at the desired ripple frequency. This bypass capacitor prevents ripple from being amplified as the output voltage is increased.

$$1/(2\pi f_{RIPPLE} * C_{ADJ}) \le R_1 \quad (1)$$

7.3.2 Load Regulation

The LM1086 regulates the voltage that appears between its output and ground pins, or between its output and adjust pins. In some cases, line resistances can introduce errors to the voltage across the load. To obtain the best load regulation, a few precautions are needed.

Figure 14 shows a typical application using a fixed output regulator. Rt1 and Rt2 are the line resistances. V_{LOAD} is less than the V_{OUT} by the sum of the voltage drops along the line resistances. In this case, the load regulation seen at the R_{LOAD} would be degraded from the data sheet specification. To improve this, the load should be tied directly to the output terminal on the positive side and directly tied to the ground terminal on the negative side.

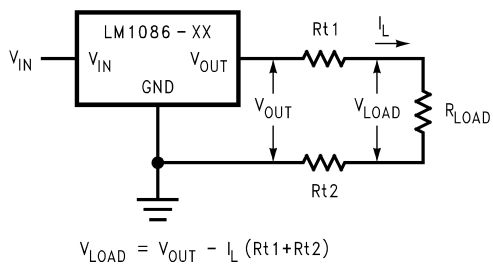


Figure 14. Typical Application Using Fixed Output Regulator

When the adjustable regulator is used (Figure 15), the best performance is obtained with the positive side of the resistor R1 tied directly to the output terminal of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 5V regulator with 0.05-Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05 Ω × I_L. If R1 (=125 Ω) is connected near the load the effective line resistance will be 0.05 Ω (1 + R2/R1) or in this case, it is 4 times worse. In addition, the ground side of the resistor R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

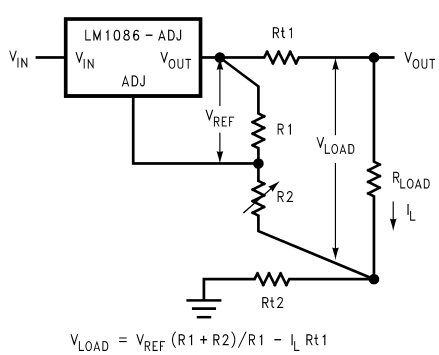


Figure 15. Best Load Regulation Using Adjustable Output Regulator

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Feature Description (continued)

7.3.3 Overload Recovery

Overload recovery refers to regulator's ability to recover from a short circuited output. A key factor in the recovery process is the current limiting used to protect the output from drawing too much power. The current limiting circuit reduces the output current as the input to output differential increases. Refer to short circuit curve in the Typical Characteristics section.

During normal start-up, the input to output differential is small since the output follows the input. But, if the output is shorted, then the recovery involves a large input to output differential. Sometimes during this condition the current limiting circuit is slow in recovering. If the limited current is too low to develop a voltage at the output, the voltage will stabilize at a lower level. Under these conditions it may be necessary to recycle the power of the regulator in order to get the smaller differential voltage and thus adequate start up conditions. Refer to Typical Characteristics section for the short circuit current vs. input differential voltage.

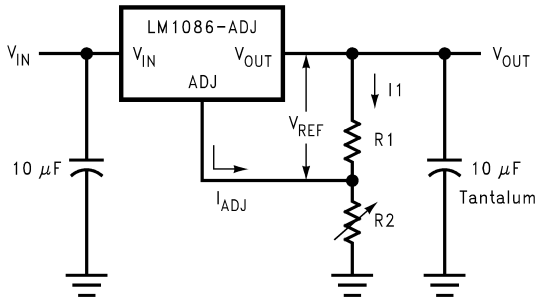
7.4 Device Functional Modes

7.4.1 Output Voltage

The LM1086 adjustable version develops a 1.25-V reference voltage, (V_{REF}), between the output and the adjust terminal. As shown in Figure 16, this voltage is applied across resistor R1 to generate a constant current I1. This constant current then flows through R2. The resulting voltage drop across R2 adds to the reference voltage to sets the desired output voltage.

The current I_{ADJ} from the adjustment terminal introduces an output error . But since it is small (120uA max), it becomes negligible when R1 is in the 100 Ω range.

For fixed voltage devices, R1 and R2 are integrated inside the devices.



$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R2$$

Figure 16. Basic Adjustable Regulator

7.4.2 Stability Consideration

Stability consideration primarily concerns the phase response of the feedback loop. In order for stable operation, the loop must maintain negative feedback. The LM1086 requires a certain amount series resistance with capacitive loads. This series resistance introduces a zero within the loop to increase phase margin and thus increase stability. The equivalent series resistance (ESR) of solid tantalum or aluminum electrolytic capacitors is used to provide the appropriate zero (approximately 500 kHz).

Aluminum electrolytics are less expensive than tantalums, but their ESR varies exponentially at cold temperatures; therefore requiring close examination when choosing the desired transient response over temperature. Tantalums are a convenient choice because their ESR varies less than 2:1 over temperature.

The recommended load/decoupling capacitance is a 10 uF tantalum or a 50 uF aluminum. These values will assure stability for the majority of applications.

The adjustable versions allows an additional capacitor to be used at the ADJ pin to increase ripple rejection. If this is done the output capacitor should be increased to 22uF for tantalum or to 150 uF for aluminum.

Capacitors other than tantalum or aluminum can be used at the adjust pin and the input pin. A 10 uF capacitor is a reasonable value at the input. See Ripple Rejection section regarding the value for the adjust pin capacitor.

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Device Functional Modes (continued)

It is desirable to have large output capacitance for applications that entail large changes in load current (microprocessors for example). The higher the capacitance, the larger the available charge per demand. It is also desirable to provide low ESR to reduce the change in output voltage:

$$\Delta V = \Delta I \times ESR \quad (2)$$

It is common practice to use several tantalum and ceramic capacitors in parallel to reduce this change in the output voltage by reducing the overall ESR.

Output capacitance can be increased indefinitely to improve transient response and stability.

7.4.3 Protection Diodes

Under normal operation, the LM1086 regulator does not need any protection diode. With the adjustable device, the internal resistance between the adjustment and output terminals limits the current. No diode is needed to divert the current around the regulator even with a capacitor on the adjustment terminal. The adjust pin can take a transient signal of ±25 V with respect to the output voltage without damaging the device.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and rate of decrease of V_{IN}. In the LM1086 regulator, the internal diode between the output and input pins can withstand microsecond surge currents of 10 A to 20 A. With an extremely large output capacitor (≥1000 µf), and with input instantaneously shorted to ground, the regulator could be damaged. In this case, an external diode is recommended between the output and input pins to protect the regulator, shown in Figure 17.

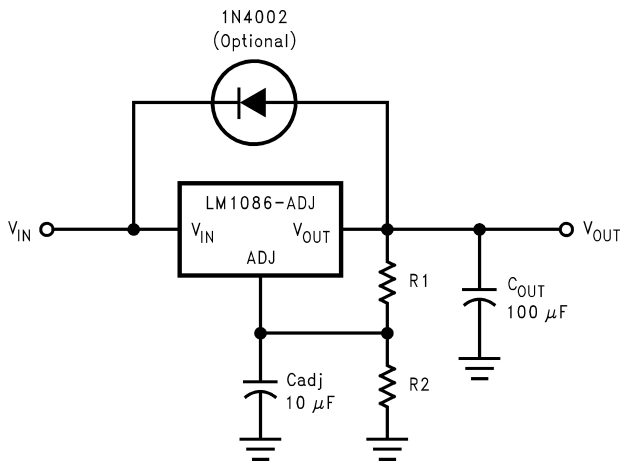

Figure 17. Regulator with Protection Diode

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM1086 is versatile in its applications, including uses in programmable output regulation and local on-card regulation. Or, by connecting a fixed resistor between the ADJUST and OUTPUT terminals, the LM1086 can function as a precision current regulator. An optional output capacitor can be added to improve transient response. The ADJUST terminal can be bypassed to achieve very high ripple-rejection ratios, which are difficult to achieve with standard three-terminal regulators. Please note, in the following applications, if ADJ is mentioned, it makes use of the adjustable version of the part, however, if GND is mentioned, it is the fixed voltage version of the part.

8.2 Typical Applications

8.2.1 1.2-V to 15-V Adjustable Regulator

This part can be used as a simple low drop out regulator to enable a variety of output voltages needed for demanding applications. By using an adjustable R2 resistor a variety of output voltages can be made possible as shown in Figure 18 based on the LM1086-ADJ.

Figure 18. 1.2-V to 15-V Adjustable Regulator

8.2.1.1 Design Requirements

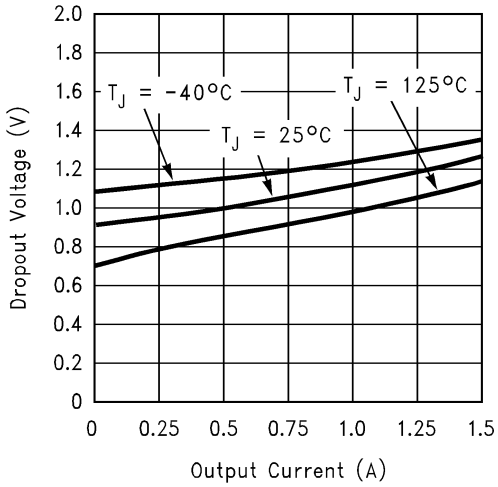
The device component count is very minimal, employing two resistors as part of a voltage divider circuit and an output capacitor for load regulation.

8.2.1.2 Detailed Design Procedure

The voltage divider for this part is set based on the equation shown in Figure 18, where R1 is the upper feedback resistor R2 is the lower feedback resistor.

Typical Applications (continued)

8.2.1.3 Application Curve



8.2.2 Adjustable at 5 V

The application shown in Figure 19 outlines a simple 5-V output application made possible by the LM1086-ADJ. This application can provide 1.5 A at high efficiencies and very low drop-out.

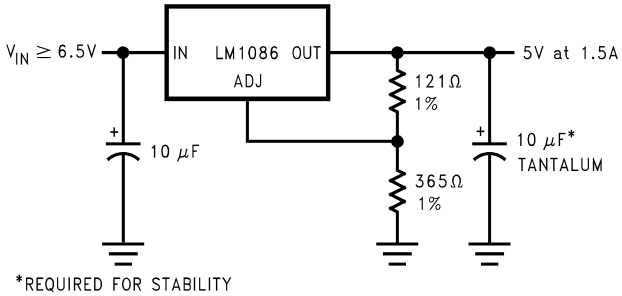


Figure 19. Adjustable at 5 V

8.2.3 5-V Regulator with Shutdown

A variation of the 5-V output regulator application with shutdown control is shown in Figure 20 based on the LM1086-ADJ. It uses a simple NPN transistor on the ADJ pin to block or sink the current on the ADJ pin. If the TTL logic is pulled high, the NPN transistor is activated and the part is disabled, outputting approximately 1.25 V. If the TTL logic is pulled low, the NPN transistor is unbiased and the regulator functions normally.

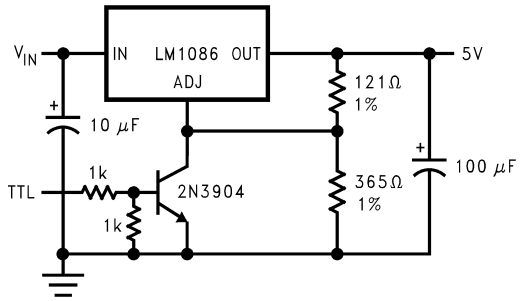


Figure 20. 5-V Regulator with Shutdown

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Typical Applications (continued)

8.2.4 Battery Charger

The LM1086-ADJ can be used as a battery charger to regulate the charging current required by the battery bank as shown in Figure 21. In this application the LM1086 acts as a constant voltage, constant current part by sensing the voltage potential across the battery and compensating it to the current voltage. To maintain this voltage, the regulator delivers the maximum charging current required to charge the battery. As the battery approaches the fully charged state, the potential drop across the sense resistor, R_S reduces and the regulator throttles back the current to maintain the float voltage of the battery.

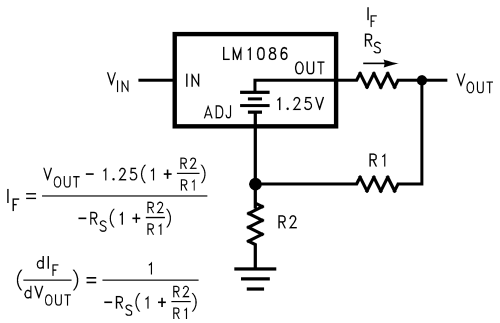

Figure 21. Battery Charger

8.2.5 Adjustable Fixed Regulator

A simple adjustable, fixed range output regulator can be made possible by placing a variable resistor on the ground of the device as shown in Figure 22 based on the fixed output voltage LM1086-5.0. The GND pin has a small quiescent current of 5 mA typical. Increasing the resistance on the GND pin increases the voltage potential across the resistor. This potential is then mirrored on to the output to increase the total output voltage by the potential drop across the GND resistor.

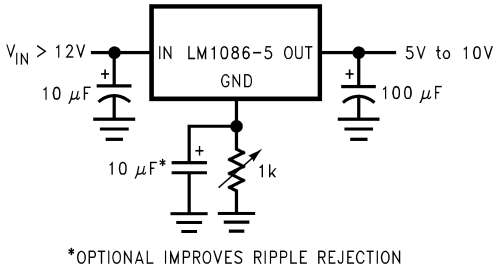

Figure 22. Adjustable Fixed Regulator

8.2.6 Regulator With Reference

A fixed output voltage version of the LM1086-5.0 can be employed to provide an output rail and a reference rail at the same time as shown in Figure 23. This simple application makes use of a reference diode, the LM136-5, to regulate the GND voltage to a fixed 5 V based on the quiescent current generated by the GND pin. This voltage is then added onto the output to generate a total of 10 V out.

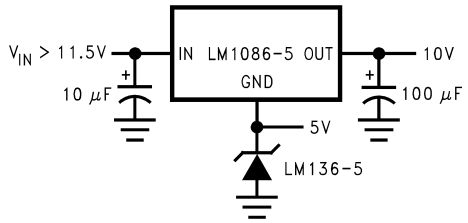

Figure 23. Regulator With Reference

Typical Applications (continued)

8.2.7 High Current Lamp Driver Protection

A simple constant current source with protection can be designed by controlling the impedance between the lamp and ground. The LM1086-ADJ shown in Figure 24 makes use of an external TTL or CMOS input to drive the NPN transistor. This pulls the output of the regulator to a few tenths of a volt and puts the part into current limit. Releasing the logic will reduce the current flow across the lamp into the normal operating current thereby protecting the lamp during startup.

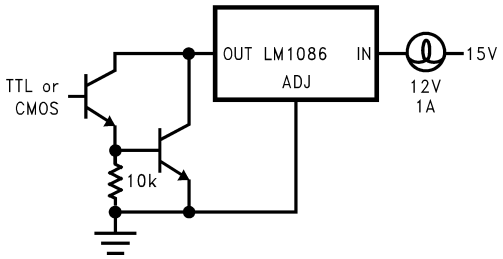

Figure 24. High Current Lamp Driver Protection

8.2.8 Battery Backup Regulated Supply

A regulated battery backup supply can be generated by using two fixed output voltage versions of the part as shown in Figure 25. The top regulator supplies the Line voltage during normal operation, however when the input is not available, the second regulator derives power from the battery backup and regulates it to 5 V based on the LM1086-5.0. The diodes prevent the rails from back feeding into the supply and batteries.

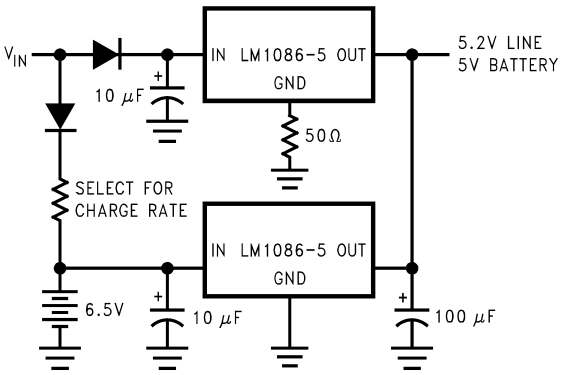

Figure 25. Battery Backup Regulated Supply

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Typical Applications (continued)

8.2.9 Ripple Rejection Enhancement

A very simple ripple rejection circuit is shown in Figure 26 using the LM1086-ADJ. The capacitor C1 smooths out the ripple on the output by cleaning up the feedback path and preventing excess noise from feeding back into the regulator. Please remember X_{C1} should be approximately equal to R1 at the ripple frequency.

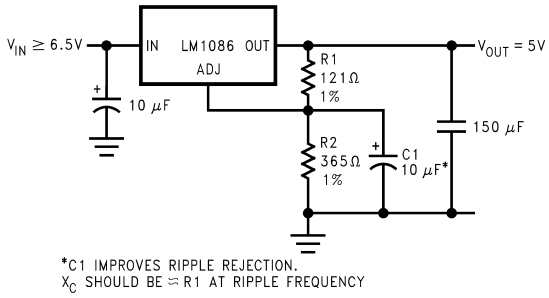

Figure 26. Ripple Rejection Enhancement

8.2.10 Automatic Light Control

A common street light control or automatic light control circuit is designed in Figure 27 based on the LM1086-ADJ. The photo transistor conducts in the presence of light and grounds the ADJ pin preventing the lamp from turning on. However, in the absence of light, the LM1086 regulates the voltage to 1.25 V between OUT and ADJ, ensuring the lamp remains on.

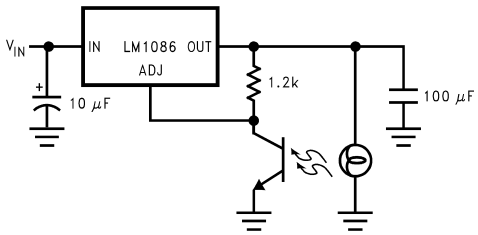

Figure 27. Automatic Light Control

8.2.11 Remote Sensing

Remote sensing is a method of compensating the output voltage to a very precise degree by sensing the output and feeding it back through the feedback. The circuit implementing this is shown in Figure 28 using the LM1086-ADJ. The output of the regulator is fed into a voltage follower to avoid any loading effects and the output of the op-amp is injected into the top of the feedback resistor network. This has the effect of modulating the voltage to a precise degree without additional loading on the output.

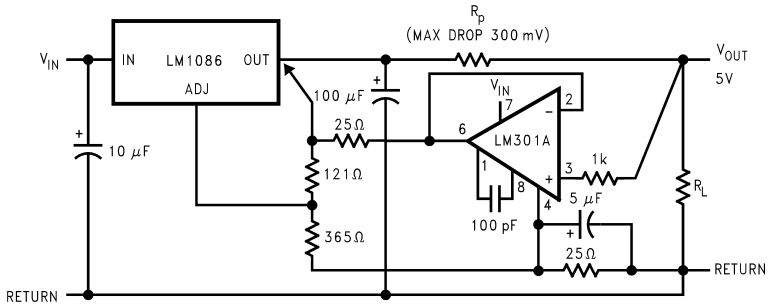

Figure 28. Remote Sensing

9 Power Supply Recommendations

The linear regulator input supply should be well regulated and kept at a voltage level such that the maximum input to output voltage differential allowed by the device is not exceeded. The minimum dropout voltage (V_{IN} – V_{OUT}) should be met with extra headroom when possible in order to keep the output well regulated. A 10 F or higher capacitor should be placed at the input to bypass noise.

10 Layout

10.1 Layout Guidelines

For the best overall performance, some layout guidelines should be followed. Place all circuit components on the same side of the circuit board and as near as practical to the respective linear regulator pins connections. Traces should be kept short and wide to reduce the amount of parasitic elements into the system. The actual width and thickness of traces will depend on the current carrying capability and heat dissipation required by the end system. An array of plated vias can be placed on the pad area underneath the TAB to conduct heat to any inner plane areas or to a bottom-side copper plane.

10.2 Layout Example

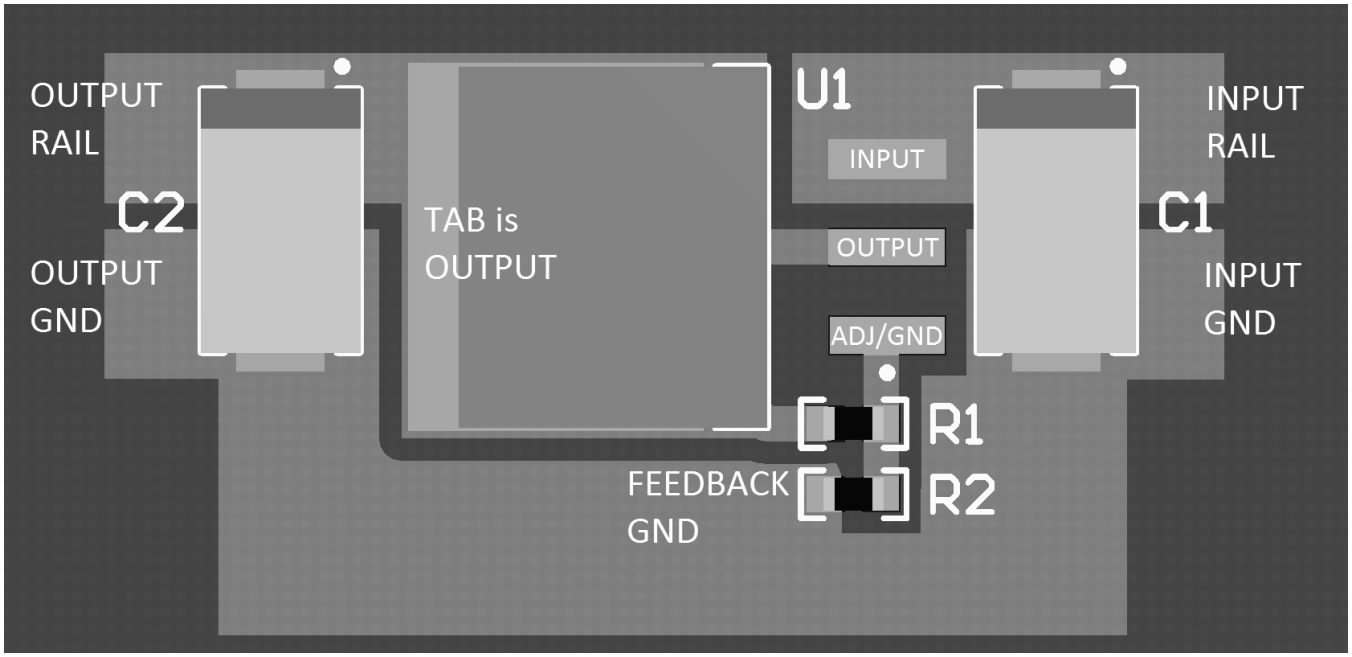

Figure 29. Layout Example

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10.3 Thermal Considerations

ICs heats up when in operation, and power consumption is one factor in how hot it gets. The other factor is how well the heat is dissipated. Heat dissipation is predictable by knowing the thermal resistance between the IC and ambient ($_{JA}$). Thermal resistance has units of temperature per power (C/W). The higher the thermal resistance, the hotter the IC.

The LM1086 specifies the thermal resistance for each package as junction to case ($_{JC}$). In order to get the total resistance to ambient ($_{JA}$), two other thermal resistance must be added, one for case to heat-sink ($_{CH}$) and one for heatsink to ambient ($_{HA}$). The junction temperature can be predicted as follows:

$$T_J = T_A + P_D (_{JC} + _{CH} + _{HA}) = T_A + P_D \ _{JA}$$

where

- T_J is junction temperature
- T_A is ambient temperature
- P_D is the power consumption of the device (3)

Device power consumption is calculated as follows:

$$I_{IN} = I_L + I_G \quad (4)$$

$$P_D = (V_{IN} – V_{OUT}) I_L + V_{IN} I_G \quad (5)$$

Figure 30 shows the voltages and currents which are present in the circuit.

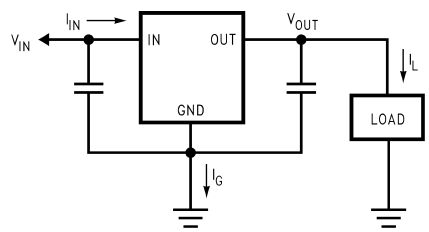

Figure 30. Power Dissipation Diagram

Once the devices power is determined, the maximum allowable ($_{JA\ (max)}$) is calculated as:

$$_{JA\ (max)} = T_{R(max)}/P_D = T_{J(max)} – T_{A(max)}/P_D$$

The LM1086 has different temperature specifications for two different sections of the IC: the control section and the output section. The Thermal Information table shows the junction to case thermal resistances for each of these sections, while the maximum junction temperatures ($T_{J(max)}$) for each section is listed in the Absolute Maximum Ratings section of the datasheet. $T_{J(max)}$ is 125°C for the control section, while $T_{J(max)}$ is 150°C for the output section.

$_{JA\ (max)}$ should be calculated separately for each section as follows:

$$_{JA}\text{ (max, CONTROL SECTION)} = (125°C - T_{A(max)})/P_D \quad (6)$$

$$_{JA}\text{ (max, OUTPUT SECTION)} = (150°C - T_{A(max)})/P_D \quad (7)$$

The required heat sink is determined by calculating its required thermal resistance ($_{HA\ (max)}$).

$$_{HA\ (max)} = _{JA\ (max)} – (_{JC} + _{CH}) \quad (8)$$

($_{HA\ (max)}$) should also be calculated twice as follows:

$$(_{HA\ (max)}) = _{JA}\text{ (max, CONTROL SECTION)} - (_{JC}\text{ (CONTROL SECTION)} + _{CH}) \quad (9)$$

$$(_{HA\ (max)}) = _{JA}\text{(max, OUTPUT SECTION)} - (_{JC}\text{ (OUTPUT SECTION)} + _{CH}) \quad (10)$$

If thermal compound is used, $_{CH}$ can be estimated at 0.2 C/W. If the case is soldered to the heat sink, then a $_{CH}$ can be estimated as 0 C/W.

After, $_{HA\ (max)}$ is calculated for each section, choose the lower of the two $_{HA\ (max)}$ values to determine the appropriate heat sink.

Thermal Considerations (continued)

If PC board copper is going to be used as a heat sink, then Figure 31 can be used to determine the appropriate area (size) of copper foil required.

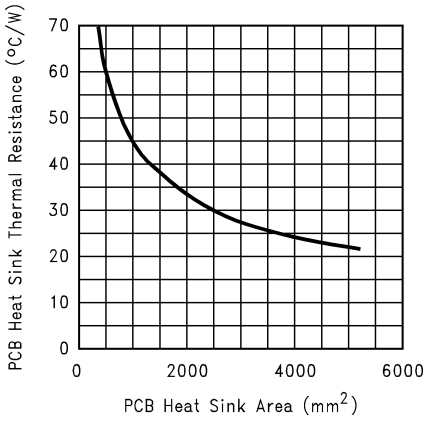

Figure 31. Heat Sink Thermal Resistance vs Area

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11 Device and Documentation Support

11.1 Development Support

For additional information, see Texas Instruments' E2E community resources at http://e2e.ti.com.

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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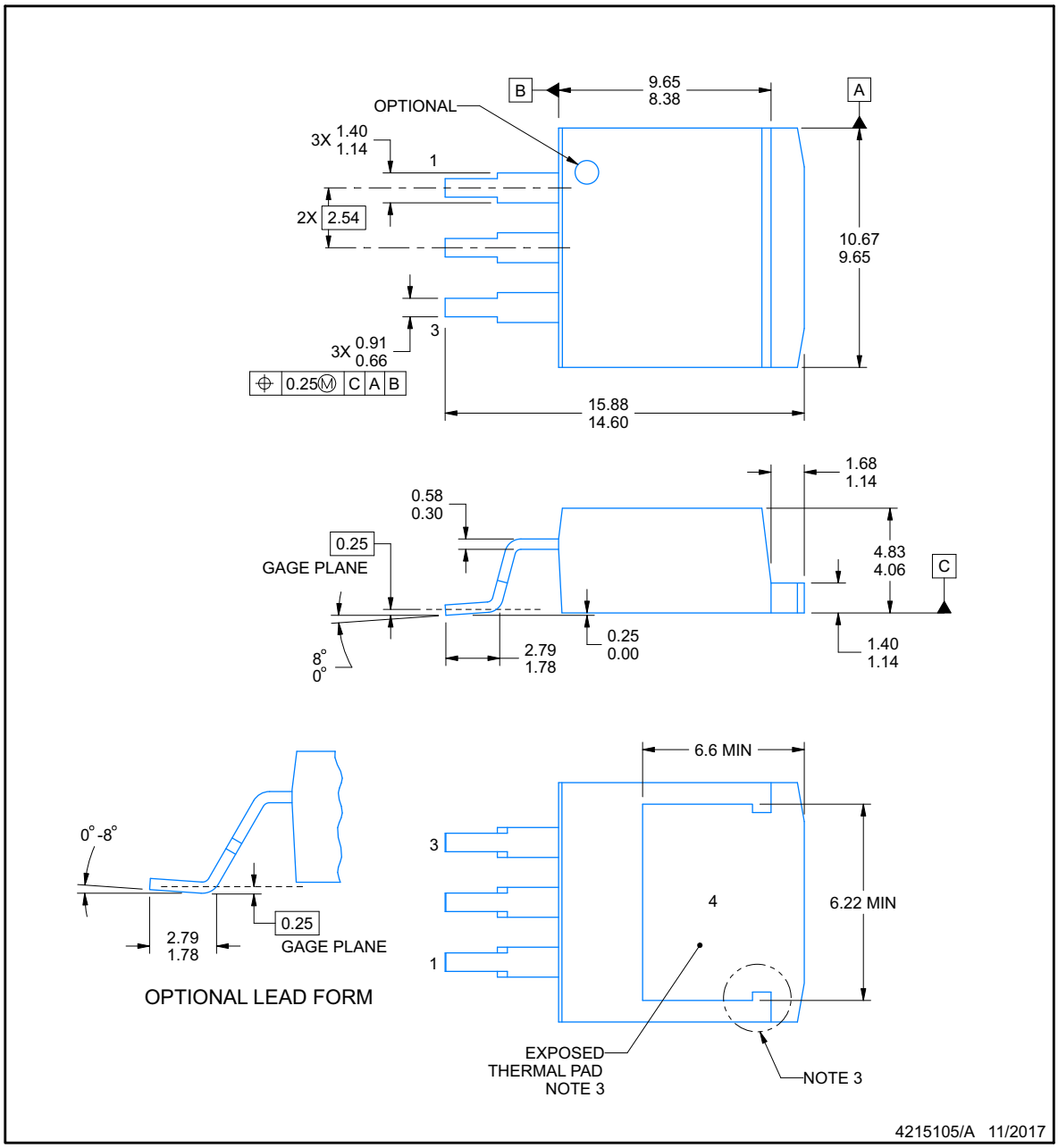
PACKAGE OUTLINE

KTT0003B

TO-263 - 4.83 mm max height

TO-263



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Features may not exist and shape may vary per different assembly sites.
4. Reference JEDEC registration TO-263, except minimum lead thickness and minimum exposed pad length.

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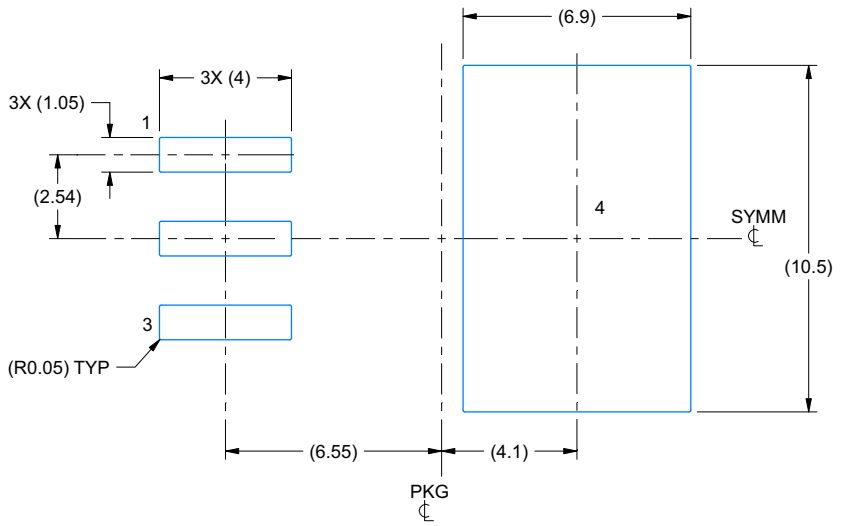
EXAMPLE BOARD LAYOUT

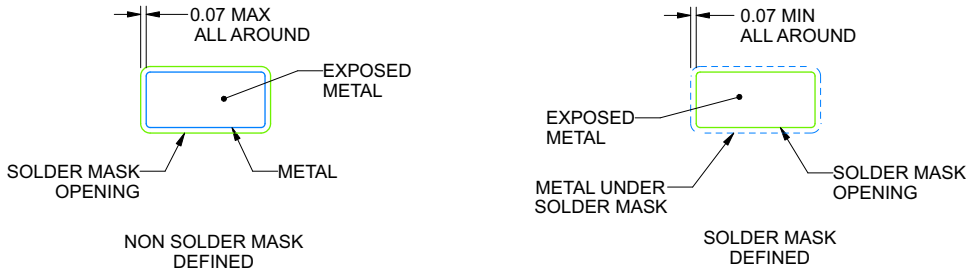
KTT0003B

TO-263 - 4.83 mm max height

TO-263



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:5X



SOLDER MASK DETAILS

4215105/A 11/2017

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

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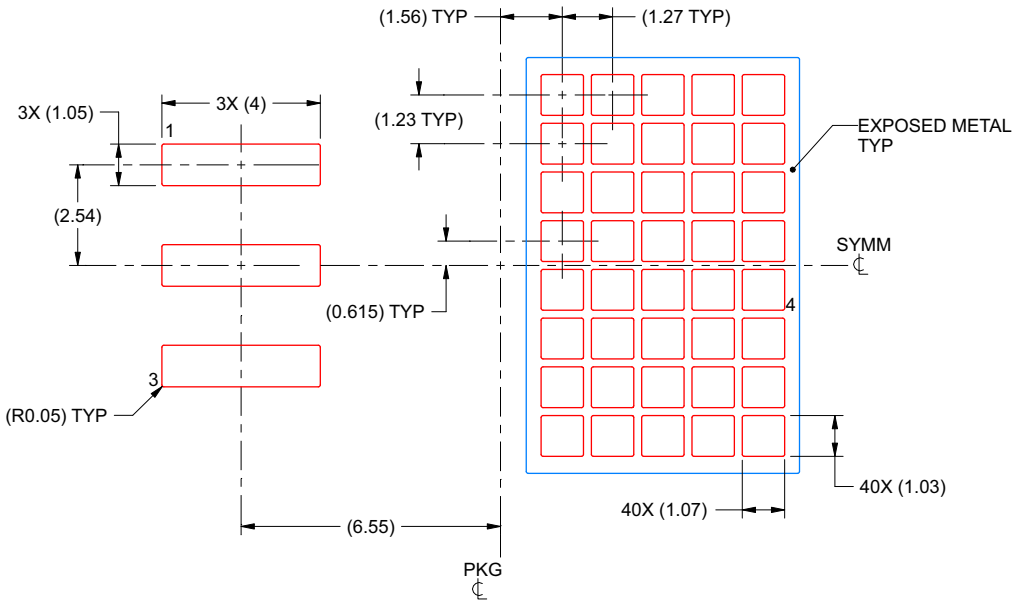
EXAMPLE STENCIL DESIGN

KTT0003B

TO-263 - 4.83 mm max height

TO-263



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
60% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

4215105/A 11/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM1086CS-2.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	0 to 125	LM1086 CS-2.5	Samples
LM1086CS-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	0 to 125	LM1086 CS-3.3	Samples
LM1086CS-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	0 to 125	LM1086 CS-5.0	Samples
LM1086CS-ADJ	NRND	DDPAK/ TO-263	KTT	3	45	Non-RoHS & Green	Call TI	Level-3-235C-168 HR		LM1086 CS-ADJ	
LM1086CS-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	0 to 125	LM1086 CS-ADJ	Samples
LM1086CSX-2.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	500	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	0 to 125	LM1086 CS-2.5	Samples
LM1086CSX-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	500	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	0 to 125	LM1086 CS-3.3	Samples
LM1086CSX-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	500	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	0 to 125	LM1086 CS-ADJ	Samples
LM1086CT-3.3/NOPB	ACTIVE	TO-220	NDE	3	45	RoHS & Green	SN	Level-1-NA-UNLIM	0 to 125	LM1086 CT-3.3	Samples
LM1086CT-5.0/NOPB	ACTIVE	TO-220	NDE	3	45	RoHS & Green	SN	Level-1-NA-UNLIM	0 to 125	LM1086 CT-5.0	Samples
LM1086CT-ADJ/NOPB	ACTIVE	TO-220	NDE	3	45	RoHS & Green	SN	Level-1-NA-UNLIM	0 to 125	LM1086 CT-ADJ	Samples
LM1086ILD-3.3/NOPB	ACTIVE	WSON	NGN	8	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	1086I33	Samples
LM1086IS-1.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LM1086 IS-1.8	Samples
LM1086IS-3.3	NRND	DDPAK/ TO-263	KTT	3	45	Non-RoHS & Green	Call TI	Level-3-235C-168 HR	-40 to 125	LM1086 IS-3.3	
LM1086IS-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LM1086 IS-3.3	Samples
LM1086IS-5.0	ACTIVE	DDPAK/ TO-263	KTT	3	45	Non-RoHS & Green	Call TI	Level-3-235C-168 HR	-40 to 125	LM1086 IS-5.0	Samples
LM1086IS-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LM1086 IS-5.0	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM1086IS-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LM1086 IS-ADJ	Samples
LM1086ISX-1.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	500	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LM1086 IS-1.8	Samples
LM1086ISX-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	500	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LM1086 IS-3.3	Samples
LM1086ISX-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	500	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LM1086 IS-5.0	Samples
LM1086ISX-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	500	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LM1086 IS-ADJ	Samples
LM1086IT-3.3/NOPB	ACTIVE	TO-220	NDE	3	45	RoHS & Green	SN	Level-1-NA-UNLIM	-40 to 125	LM1086 IT-3.3	Samples
LM1086IT-5.0/NOPB	ACTIVE	TO-220	NDE	3	45	RoHS & Green	SN	Level-1-NA-UNLIM	-40 to 125	LM1086 IT-5.0	Samples
LM1086IT-ADJ/NOPB	ACTIVE	TO-220	NDE	3	45	RoHS & Green	SN	Level-1-NA-UNLIM	-40 to 125	LM1086 IT-ADJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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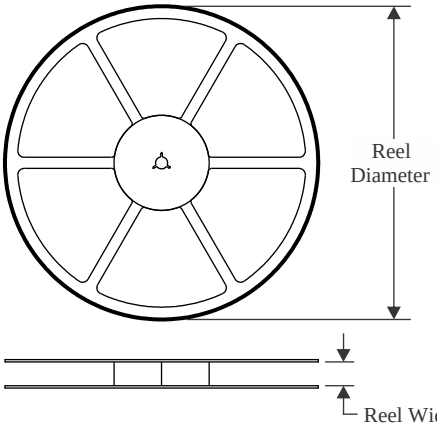
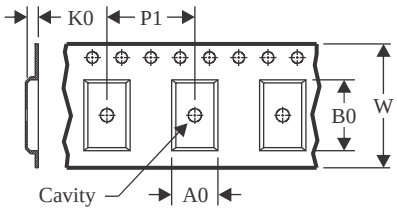
TAPE AND REEL INFORMATION

REEL DIMENSIONS

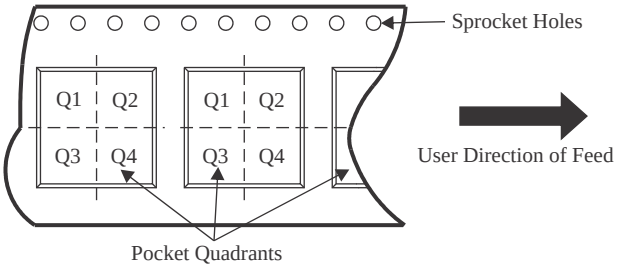


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

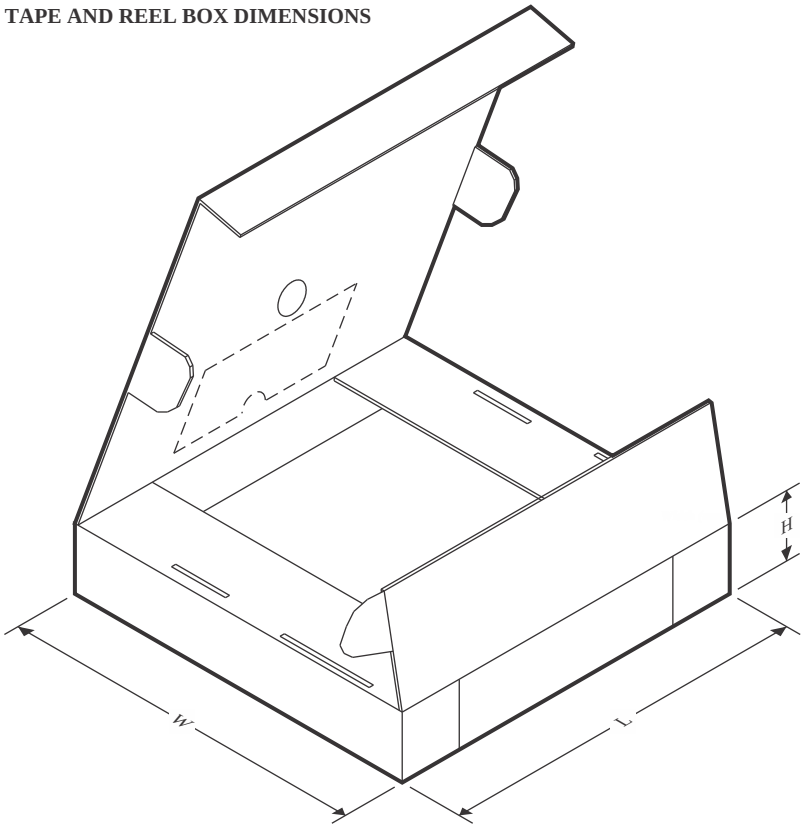
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM1086CSX-2.5/NOPB	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM1086CSX-3.3/NOPB	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM1086CSX-ADJ/NOPB	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM1086ILD-3.3/NOPB	WSON	NGN	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM1086ISX-1.8/NOPB	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM1086ISX-3.3/NOPB	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM1086ISX-5.0/NOPB	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM1086ISX-ADJ/NOPB	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

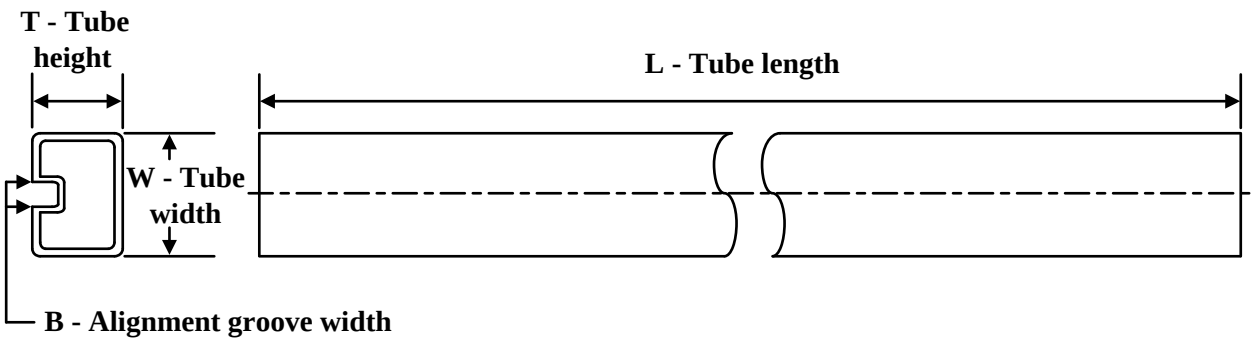
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM1086CSX-2.5/NOPB	DDPAK/TO-263	KTT	3	500	367.0	367.0	45.0
LM1086CSX-3.3/NOPB	DDPAK/TO-263	KTT	3	500	367.0	367.0	45.0
LM1086CSX-ADJ/NOPB	DDPAK/TO-263	KTT	3	500	367.0	367.0	45.0
LM1086ILD-3.3/NOPB	WSON	NGN	8	1000	208.0	191.0	35.0
LM1086ISX-1.8/NOPB	DDPAK/TO-263	KTT	3	500	367.0	367.0	45.0
LM1086ISX-3.3/NOPB	DDPAK/TO-263	KTT	3	500	367.0	367.0	45.0
LM1086ISX-5.0/NOPB	DDPAK/TO-263	KTT	3	500	367.0	367.0	45.0
LM1086ISX-ADJ/NOPB	DDPAK/TO-263	KTT	3	500	367.0	367.0	45.0

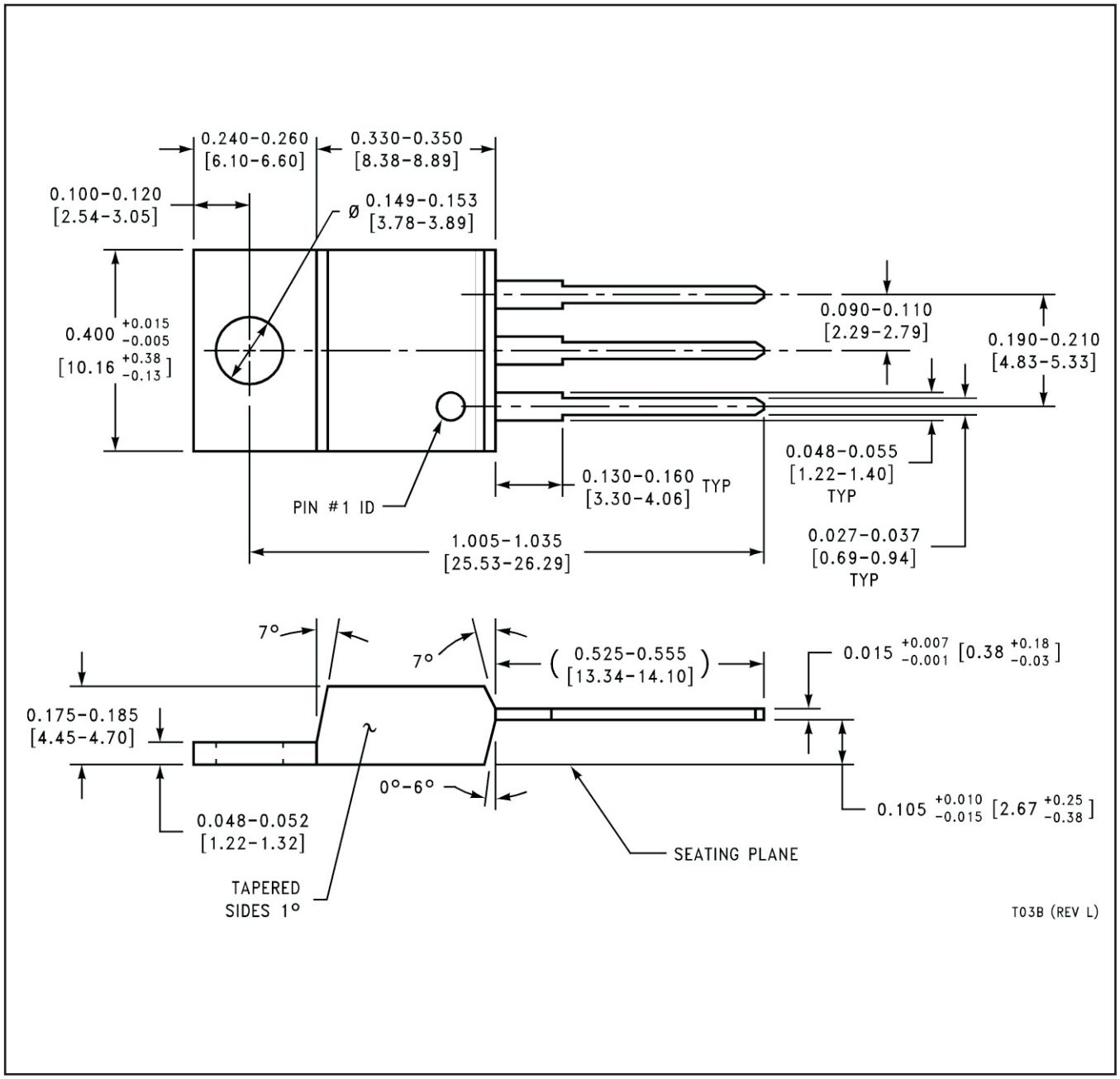
TUBE

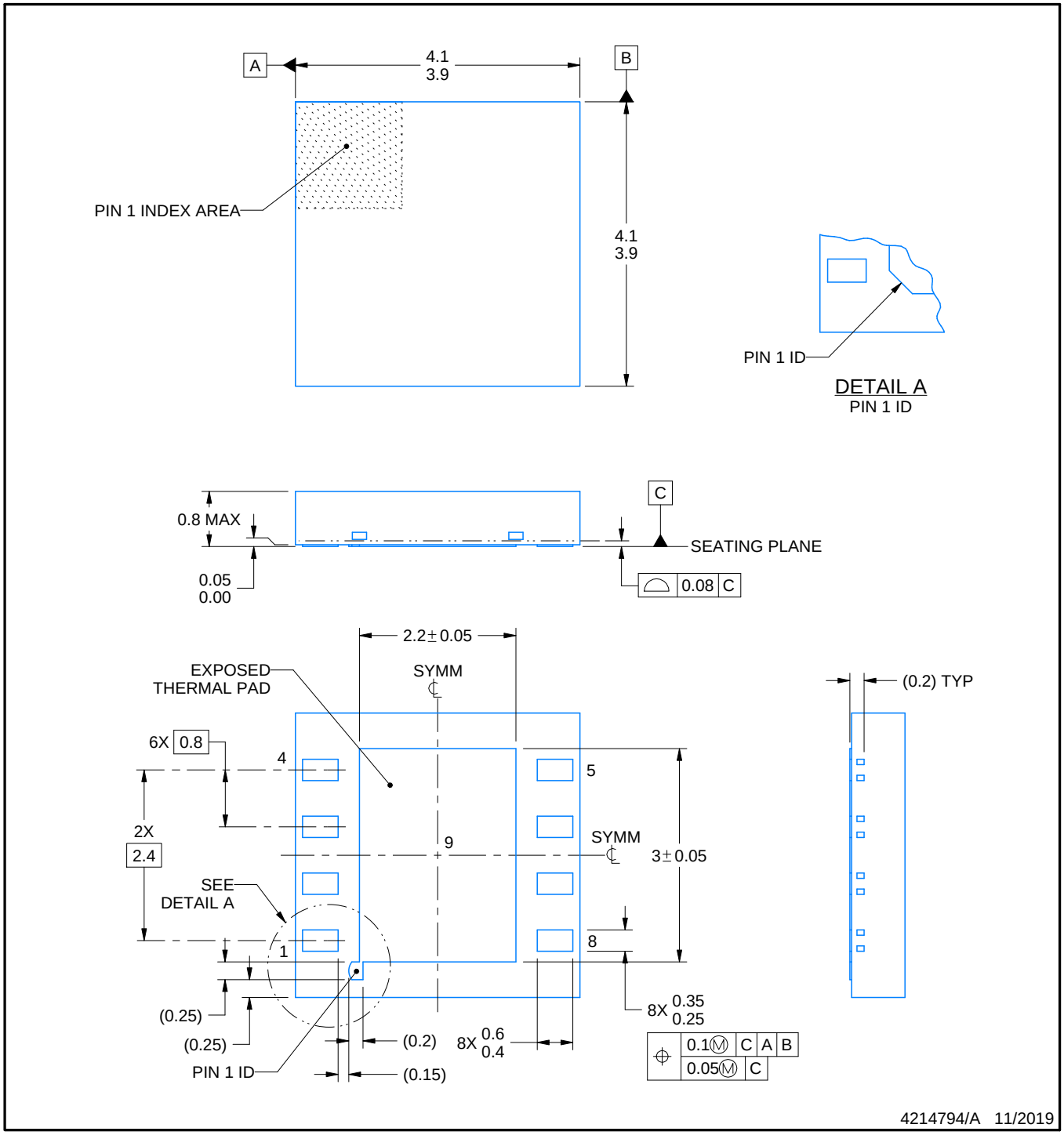


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM1086CS-2.5/NOPB	KTT	TO-263	3	45	502	25	8204.2	9.19
LM1086CS-3.3/NOPB	KTT	TO-263	3	45	502	25	8204.2	9.19
LM1086CS-5.0/NOPB	KTT	TO-263	3	45	502	25	8204.2	9.19
LM1086CS-ADJ	KTT	TO-263	3	45	502	25	8204.2	9.19
LM1086CS-ADJ	KTT	TO-263	3	45	502	25	8204.2	9.19
LM1086CS-ADJ/NOPB	KTT	TO-263	3	45	502	25	8204.2	9.19
LM1086CT-3.3/NOPB	NDE	TO-220	3	45	502	33	6985	4.06
LM1086CT-5.0/NOPB	NDE	TO-220	3	45	502	33	6985	4.06
LM1086CT-ADJ/NOPB	NDE	TO-220	3	45	502	33	6985	4.06
LM1086IS-1.8/NOPB	KTT	TO-263	3	45	502	25	8204.2	9.19
LM1086IS-3.3	KTT	TO-263	3	45	502	25	8204.2	9.19
LM1086IS-3.3	KTT	TO-263	3	45	502	25	8204.2	9.19
LM1086IS-3.3/NOPB	KTT	TO-263	3	45	502	25	8204.2	9.19
LM1086IS-5.0	KTT	TO-263	3	45	502	25	8204.2	9.19
LM1086IS-5.0	KTT	TO-263	3	45	502	25	8204.2	9.19
LM1086IS-5.0/NOPB	KTT	TO-263	3	45	502	25	8204.2	9.19
LM1086IS-ADJ/NOPB	KTT	TO-263	3	45	502	25	8204.2	9.19
LM1086IT-3.3/NOPB	NDE	TO-220	3	45	502	33	6985	4.06
LM1086IT-5.0/NOPB	NDE	TO-220	3	45	502	33	6985	4.06
LM1086IT-ADJ/NOPB	NDE	TO-220	3	45	502	33	6985	4.06

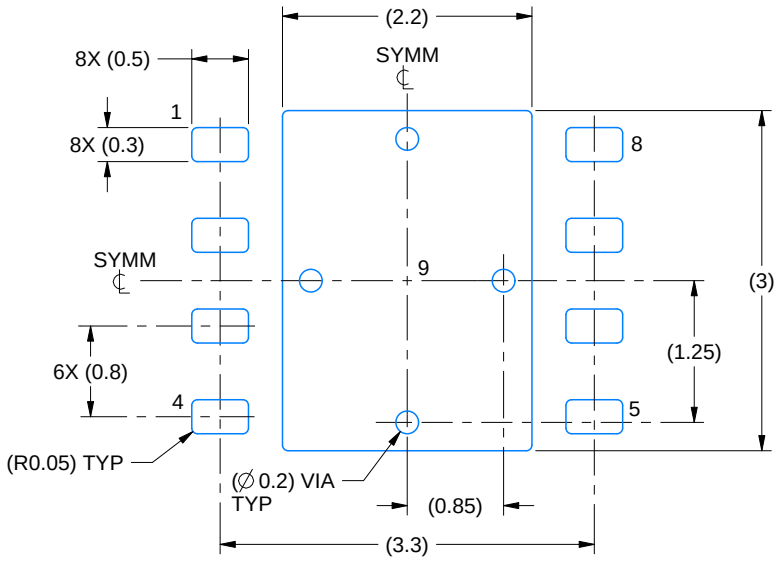
NDE0003B


0.240-0.260
[6.10-6.60]
0.330-0.350
[8.38-8.89]
0.100-0.120
[2.54-3.05]
Ø 0.149-0.153
[3.78-3.89]
0.400 +0.015 -0.005
[10.16 +0.38 -0.13]
0.090-0.110
[2.29-2.79]
0.190-0.210
[4.83-5.33]
0.048-0.055
[1.22-1.40]
TYP
0.130-0.160 TYP
[3.30-4.06]
PIN #1 ID
1.005-1.035
[25.53-26.29]
0.027-0.037
[0.69-0.94]
TYP
7°
7°
(0.525-0.555)
[13.34-14.10]
0.015 +0.007 -0.001 [0.38 +0.18 -0.03]
0.175-0.185
[4.45-4.70]
0°-6°
0.105 +0.010 -0.015 [2.67 +0.25 -0.38]
0.048-0.052
[1.22-1.32]
SEATING PLANE
TAPERED
SIDES 1°
T03B (REV L)

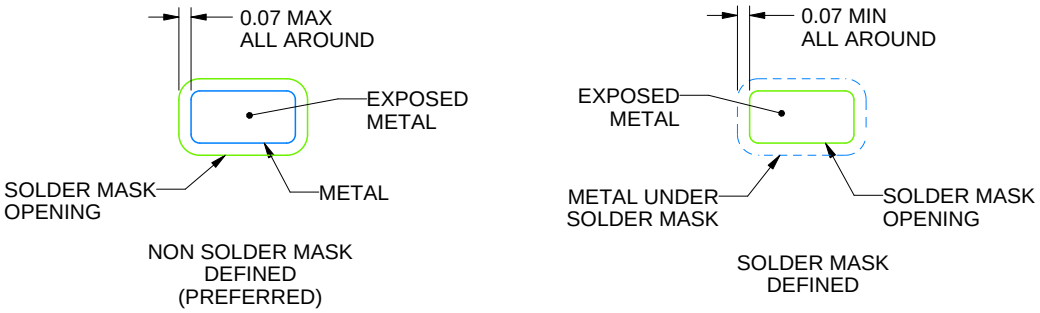


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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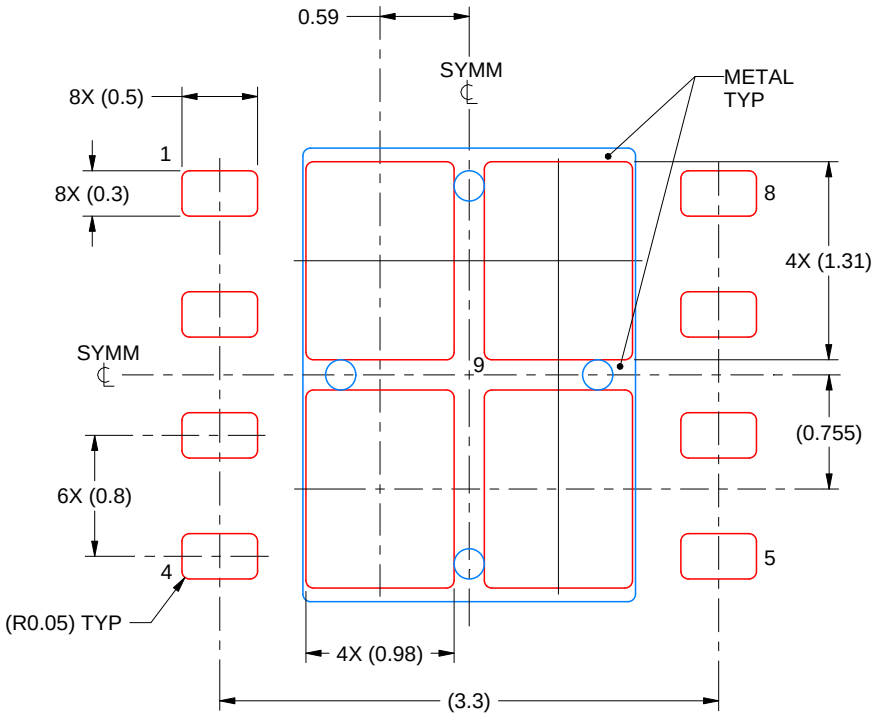
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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